

ABSTRACT OF THE DISCLOSURE

A field effect transistor of the present invention is formed in a strain effect semiconductor layer, represented by a strain effect silicon layer, formed in an upper layer of a semiconductor substrate. A source/a drain of the field effect transistor are formed only in the strain effect silicon layer. The field effect transistor may be formed as an nMOS transistor, and a pMOS transistor may be formed in the strain effect silicon layer while being isolated from the nMOS transistor through an isolation region. A logic circuit can be formed of these transistors. Although when an nMOS transistor or a pMOS transistor is employed in an application requiring a high performance at a low voltage, there occurs a current leak because the junction of a source/a drain is positioned in a silicon germanium layer having a low band gap or formed at an interface of silicon/silicon germanium, the field effect transistor of the present invention prevents occurrence of such a current leak.